

Requirements for ADC in high-speed optical modules



Overview

Several technologies and design considerations are crucial for ADC performance in optical modules: Sampling Rate and Clock Jitter: High-speed ADCs require stable, low-jitter clock signals. Clock jitter affects ENOB (Effective Number of Bits) and limits achievable SNR. The ADC chips for optical communication systems are critical components that enable accurate, high-speed conversion of optical signals into digital electrical signals for processing. However, the ultra-short (less than tens of pico-seconds) post-sampling pulse. ABSTRACT Electrical-optical signal processing has been shown to be a promising path to overcome the limitations of state-of-the-art all-electrical data converters. In addition to ultra-broadband signal processing, it allows leveraging ultra-low jitter mode-locked lasers and thus increasing the. Whilst commercial oscilloscopes provide high sampling rates, they present significant limitations for quantum research: they offer limited channel counts, lack distributed synchronisation capabilities, and become prohibitively expensive when scaled to multi-channel configurations required for. The goal of this document is to introduce a wide range of theories and topics that are relevant to high-speed, analog-to-digital converters (ADC). This document provides details on sampling theory, data-sheet specifications, ADC selection criteria and evaluation methods, clock jitter, and other. Our high-speed analog-to-digital converter (ADC) portfolio offers solutions for high speed conversion applications including aerospace, defense, wireless, industrial and test.

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The ADC chip in an optical module | Weyland

As optical networks move toward higher data rates and denser deployment, ADCs will continue to evolve with higher

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CMOS ADCs for Optical Communications | Springer Nature Link

This paper provides a systematic view of ADCs embedded in DSP receivers of coherent optical communications

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